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Radio Front End - Baseband Digital Parallel (RBDP) Interface

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RADIO FRONT END-BASEBAND DIGITAL PARALLEL (RBDP) INTERFACE

Foreword

This standard establishes the requirements for a RF-BB Digital Parallel (RBDP) interface between a Radio Front-end integrated circuit (RFIC) and a BaseBand (BBIC) integrated circuit. The interface definition includes both data path transfers and control plane transactions. Included are requirements for electrical/physical signaling and logical/functional operation. These requirements are intended to ensure that multiple RFIC and BBIC components can interoperate across a common IC interface.

Introduction

This interface definition is intended for applications where the RFIC and BBIC are mounted on the same PCB, connected by relatively short PCB traces. A typical example would be a wireless networking NIC realized on a PCMCIA ExpressCard or Mini-PCI card format.

1.1 Data Path Overview

The data path interface is a (relatively) low-speed parallel-bus digital interface that has been defined primarily for wireless networking applications, transferring baseband I and Q waveform digital data samples in both directions between the BBIC and RFIC. The design envelope for the data path interface includes system configurations with both one and two RF/antenna paths in each direction : specifically, this includes 1T1R, 1T2R and 2T2R systems.

The data path interface consists of fourteen or sixteen single-ended LVCMOS digital signals, including clocks, control signals and data bus signals. The data bus width is matched to the baseband sample width being used : 10-bit sample widths are mandatory while 12-bit sample widths are optional. The data bus is bi-directional and alternates between transmit and receive transfer bursts, so the interface definition supports TDD or half-duplex FDD wireless networking system operation. The clock rates and interface transfer speeds support system architectures with up to 2x Nyquist over-sampling (including 802.16 WiMAX “sampling factor” expansion) for 20MHz channel bandwidths for up to 2 RF/antenna paths within the RFIC.

Figure 1 illustrates the RBDP data path interface.

1.2 Data Path Features

1. Data path clock and data rate controlled by RFIC (configured by BBIC) up to 90 MHz and 180 MSps
2. Data width matched to baseband sample width – 10 or 12 bits
3. Raw data path interface transfer bandwidth up to 1.8 or 2.2 Gbps
4. Double data rate (DDR) source-synchronous data path transfer timing
5. Low latency (single baseband complex sample period) data transfer
6. Low implementation complexity
7. Low power idle modes

1.3 Control Plane Overview

The control plane interface consists of three or four single-ended LVCMOS digital signals, including clock, chip-select and 1-bit serial data signals. The data signaling can be implemented either as two separate unidirectional signals or as a single bi-directional signal, but whichever is used, the data transfer is always half-duplex. The interface definition supports non-overlapping memory-mapped register read or write transactions with 8b-wide data fields. An extended transaction format allows multiple data fields to be transferred in a single transaction, reducing overhead and increasing efficiency and throughput.

Figure 2 illustrates the control plane board-level connections for the RBDP interface.

1.4 Control Plane Features

1. Clock rate and serial transfer rate controlled by BBIC up to 50 MHz
2. 1-bit command + 7-bit address control field format
3. Flexible transaction format using one or more 8-bit data fields per transaction allows per-transaction optimization of latency or bandwidth
 - a. minimum 325ns transaction latency with 8-bit data transactions (maximum 24 Mbps data rate)
 - b. data rates above 40 Mbps can be achieved with extended transactions (see section 5.2.2)
4. Serial clock can be stopped between transactions, reducing control plane power consumption to negligible levels

RADIO FRONT END–BASEBAND DIGITAL PARALLEL (RBDP) INTERFACE

(From JEDEC Board Ballot JCB-07-18, formulated under the cognizance of the JC-61 Committee on Wireless Interface Network.)

1 Scope

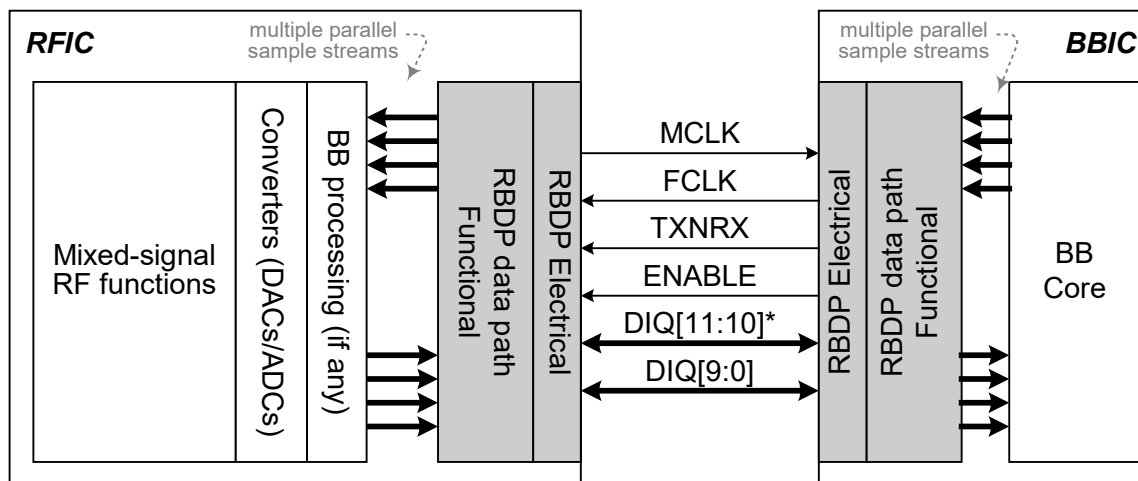
The normative information in this standard is intended to provide a technical design team to implement data path and control plane interface functions for an RFIC component and/or a BBIC component such that these components will operate correctly with each other (at the interface level), when designed to this specification. Additional information is provided in the annexes to help illustrate the normative material.

This document addresses the following interface topics for each of the data path and control plane definitions :

- 1) Electrical : time and amplitude specifications for individual signal transitions and related groups of signal transitions;
- 2) Functional : data path transfer burst format and control plane transaction format

This document defines a parallel data path and a serial control plane which together enable the bi-directional transfer of data and control/status information between the RFIC and the BBIC. The interface definition covers electrical signaling, digital timing, bit ordering and field formatting requirements to promote basic interoperability between multiple vendors. The interface definition does not extend to the level of automatic discovery of component capabilities which would be required to enable true “plug-n-play” operation.

Figure 1 illustrates the data path board-level connections and the layering of functions described by this interface definition (in the gray-shaded boxes) as well as a conceptual view of the internal connections for the interface logic blocks within the RFIC and BBIC.

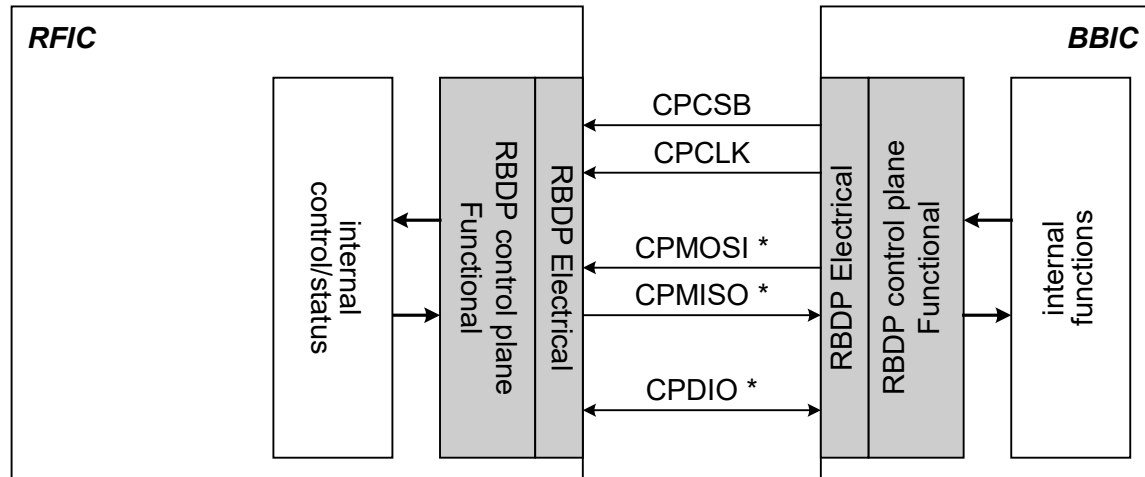


* DIQ[11:10] are optional, implemented if support for 12-bit baseband sample widths is required.

Figure 1 — RBDP interface data path signals and layers

1 Scope (cont'd)

Figure 2 illustrates the control plane board-level connections and the layering of functions described by this interface definition (in the gray-shaded boxes) as well as a conceptual view of the internal connections for the interface logic blocks within the RFIC and BBIC.



* The serial data transfer may be implemented using a single bidirectional pin CPDIO instead of two unidirectional pins CPMOSI and CPMISO.

Figure 2 — RBDP interface control plane signals and layers

2 References

Informative

The following standards contain provisions that, through references in the text, are informative in this standard. At the time of publication, the editions indicated were valid. All standards are subject to revisions.

<latest versions of 802.11 and 802.16 at time of publication>.

Normative

JESD76, *Description of 1.8 V CMOS Logic Devices*, April 2000

JESD8-7A, *1.8 V \pm 0.15 V (Normal Range) and 1.2 V - 1.95 V (Wide Range) Power Supply Voltage and Interface Standard for Nonterminated Digital Integrated Circuits*, October 2001

3 Terminology

For the purpose of this standard, the following terms, definitions, acronyms and abbreviations apply.

3.1 Terms and definitions

baseband frequencies: Low frequencies neighboring and including 0 Hz. These frequencies are represented with real In-Phase (I) and Quadrature (Q) parts or together as a complex signal. In this document, the word “baseband” will usually refer to a baseband processor (part of the BBIC in this interface).

(baseband) complex sample: one related pair of I and Q data words for one radio path, Q following I consecutively across the data path interface

complex sample rate: the minimum FFT sample rate required to support the system’s radio channel bandwidth. Defined by the wireless networking PHY standard concerned: e.g., 802.11 (= 2x Channel Bandwidth) or 802.16 (2x Sampling Factor x Channel Bandwidth). See Annex A for an illustration of applications of this interface definition and resulting sample rates, data rates and clock frequencies.

control plane transaction: a sequence of signal transitions on the control plane interface such that a single complete control plane read or write operation is executed

deskew: The act of aligning a clock with incoming data so that the clock edge can be used to latch data in the middle of the data eye.

data plane transfer burst: a sequence of transitions on the data plane signals which results in one or more baseband sample being communicated in either direction between the RFIC and the BBIC

interface baseband sample rate: the rate at which complex samples are transferred across the data path interface. May be either 1x, 2x or 4x the complex sample rate, depending upon system configuration. See Annex A for an illustration of applications of this interface definition and resulting sample rates, data rates and clock frequencies.

interface data rate (per pin): the number of bits transferred per DIQ signal per second. Must always be at least 2x, 4x or 8x the complex sample rate, depending upon system configuration.

radio: A device or a group of devices that translates the information bandwidth between baseband and the radio frequency portion of the spectrum.

sample: one data word, either I or Q, transferred across the data path interface.

receive direction: Direction of data flow across the interface, from the RFIC to the BBIC.

transmit direction: Direction of data flow across the interface, from the BBIC to the RFIC.

3 Terminology (cont'd)

3.2 Acronyms and abbreviations

BBIC	Baseband integrated circuit. May also include other functions beyond the wireless networking PHY baseband DSP functions which process the data samples transferred by the data path interface defined by this document.
BW	Bandwidth
DDR	Double data rate clocking. Data captured on both the rising and falling edges of the interface clock signal. Also known as “both-edge” clocking.
MAC	Medium Access Control layer of a Wireless LAN, MAN or PAN standard
PHY	A Wireless LAN, MAN or PAN standard physical layer interface . The bottom layer of the JC-61 RF-BB is called “electrical layer”.
RF	Relating to a Radio Frequency device.
RFIC	Radio Front-end integrated circuit. May also include some digital baseband processing, and must include the data converters (ADCs/DACs) which process the data samples transferred by the data path interface defined by this document.
Rx	Receive
SDO, SDI	Serial Data Out, Serial Data In
ToF	Time of Flight delay; propagation time of a signal on a PCB trace.
Tr	Rising or falling transition time. The time it takes to transition from one defined signal level to another.
Tx	Transmit
UI	Unit interval or bit interval. For double data rate clocking, the unit interval is half of a clock cycle.
WLAN	Wireless data packet Local Area Network in a general sense, including IEEE 802.11, wireless Metropolitan Area Networks, including IEEE 802.16; and wireless Personal Area Networks, including IEEE 802.15.

3.3 Numeric representation

The numerical values are in decimal unless indicated otherwise. The values specified in decimal are coded in natural binary unless otherwise stated. Hexadecimal values are formatted as “0xHHHH”.

4 Data path Functional layer

The RBDP data path interface definition uses bidirectional bursts to transfer groups of data samples between the RFIC and BBIC. The burst transfers are controlled using simple hardware handshake signaling. The BBIC is the interface controller, initiating and terminating all data transfer bursts.

The data path interface uses clock-looping and source-synchronous capture timing to support the highest interface transfer rates.

Some example interface applications and resulting interface data rates are shown in Annex A ,including statements of which frequencies and data rates are mandatory and which are optional.

4.1 Data path signals

The data path interface consists of the following signals.

4.1.1 MCLK (Driven from RFIC to BBIC)

Provides the primary controlling clock as the timing reference for the interface data transfers and for the baseband processing of the data samples. Provides source-synchronous timing with both edge capture for the DIQ[9:0] signals during receive bursts.

MCLK frequency depends upon the system architecture (number of RF/antenna paths and degree of over-sampling). Some example applications and resulting sample/data/clock rates are given in Annex A.

MCLK can optionally be stopped by the RFIC (in response to a control plane transaction from the BBIC) during interface idle periods to reduce power consumption. If MCLK is stopped, the transition to and from the non-toggling state must obey the electrical layer requirements for clean signal transitions, and a valid level must be driven by the RFIC at all times. The RFIC should provide a specification for settling latency when the clock is re-started (also in response to a control plane transaction from the BBIC). This latency specification is outside the scope of this standard.

4.1.2 FCLK (Driven from BBIC to RFIC)

Provides source-synchronous timing with rising edge capture for the burst control signals. Provides source-synchronous timing with both edge capture for the DIQ signals during transmit bursts. For lower interface rates, the RFIC may choose not to use FCLK if it can satisfy equivalent timing constraints to those given in section 4.3 using an internal clock.

FCLK is nominally generated by looping the BBIC's MCLK input back out again to the RFIC. Other implementations which meet the frequency-locked and phase-relationship constraints between the MCLK output and the FCLK input at the RFIC are possible. The loop delay through the BBIC from MCLK input to FCLK output must meet a loop delay constraint given in section 4.3.3. This constraint ensures that the RFIC can deterministically transfer burst control and data signals from the FCLK domain into its internal MCLK domain, and hence allows the interface to have deterministic transfer latencies.

FCLK can optionally be stopped by the BBIC during interface idle periods to reduce power consumption. If so, the transitions to and from the non-toggling state must obey the electrical layer requirements for clean signal transitions, and a valid level must be driven by the BBIC at all times. If FCLK is stopped, it must be restarted at least one complete cycle before any signal transitions that must be sampled into the RFIC by FCLK. The RFIC may impose an implementation latency requirement of more than one complete cycle from FCLK restart before input signal transitions will be correctly sampled.

4.1 Data path signals (cont'd)

4.1.3 TXNRX (Driven from BBIC to RFIC)

Provides data transfer burst control (along with ENABLE). The level on TXNRX controls the direction of the transfer burst. Sampled by the RFIC using FCLK rising edge.

The TXNRX input is qualified by the ENABLE input : when ENABLE is sampled high by the RFIC to start a burst, the level on TXNRX is also sampled and indicates the burst direction. TXNRX sampled high indicates a transmit burst; TXNRX sampled low indicates a receive burst.

The TXNRX signal level must be maintained throughout a data transfer burst. The TXNRX signal may be established any number of cycles (≥ 0) before the ENABLE start pulse is sampled, and may be changed any number of cycles (≥ 0) after the ENABLE finish pulse is sampled. The RFIC may impose an implementation-dependent requirement for TXNRX to be established some specific number of cycles before the ENABLE start pulse and to be maintained some specific number of cycles after the ENABLE finish pulse.

This behavior is further described in Annex B.

4.1.4 ENABLE (Driven from BBIC to RFIC)

Provides data transfer burst control (along with TXNRX). Asserted by the BBIC for a single cycle to indicate the start of each burst, and subsequently asserted a second time for a single cycle to indicate the end of each burst. Sampled by the RFIC using FCLK rising edge.

The RFIC must internally track the sequence of ENABLE pulses to correctly interpret each pulse as either the start or finish of each burst. The level sampled on TXNRX during each ENABLE start pulse controls the burst direction. The start and finish latencies (between the ENABLE pulses being sampled by the RFIC and the presence of the first and last valid data samples on the DIQ[9:0] bus) are shown in the timing diagrams in section 4.3.

The minimum spacing between ENABLE start and finish pulses is two FCLK cycles (i.e. the minimum data transfer burst length is two complex samples (2x I,Q pairs). The maximum burst length limit is not specified.

The minimum spacing between ENABLE finish and start pulses (i.e. the minimum gap between bursts) is not specified, but will be an implementation-dependent constraint in either the BBIC or the RFIC.

This behavior is further described in Annex B.

4.1 Data path signals (cont'd)

4.1.5 DIQ[11:10], DIQ[9:0] (Bidirectional)

Carries the data samples being transferred between BBIC and RFIC. Sampled by the RFIC using FCLK (both edges) during a transmit burst, and by the BBIC using MCLK (both edges) during a receive burst.

DIQ[11:10] are optional, used to support 12-bit sample width for applications requiring greater data sample dynamic range. Support of 10-bit sample width and DIQ[9:0] is mandatory. In this interface definition, description of DIQ[9:0] function, operation and timing behavior includes DIQ[11:10] if present.

During a transmit burst, the DIQ bus is driven by the BBIC such that the setup and hold times between FCLK and DIQ[9:0] arriving at the RFIC enable the RFIC to use FCLK to capture DIQ[9:0]. The burst start and burst finish latencies (between the ENABLE pulses being sampled by the RFIC and the presence of the first and last valid data samples on the DIQ[9:0] bus) are shown in the timing diagrams in section 4.3.

During a receive burst, the DIQ bus is driven by the RFIC such that the setup and hold times between MCLK and DIQ[9:0] arriving at the BBIC enable the BBIC to use MCLK to capture DIQ[9:0]. The burst start and burst finish latencies (between the ENABLE pulses being sampled by the RFIC and the presence of the first and last valid data samples on the DIQ[9:0] bus) are shown in the timing diagrams in section 4.3.

The data samples are carried in two's complement format, with DIQ[9] (or DIQ[11] if present) as the numerically most significant bit and DIQ[0] as the least significant bit.

e.g., the most positive sample value is 0x1ff (or 0x7ff), and the most negative value is 0x200 (or 0x800).

The I and Q data samples are time-interleaved on the DIQ bus. For a single RF/antenna path in each direction (i.e., a 1T1R system), the I and Q samples are carried in a 2-way interleave.

e.g., I, Q, I, Q, ...

For a system with two paths in each direction (i.e. a 2T2R system), the I and Q samples from RF/antenna path A and B are carried in a 4-way interleave.

e.g., I_A, Q_A, I_B, Q_B, I_A, Q_A, I_B, Q_B, ...

For a system with asymmetrical transmit and receive paths such as a 1T2R system, the clock frequencies, bus transfer rates and sample periods, and data capture timing are all as for the 2T2R system case. However, in one direction the second half of each group of sample periods on the bus will be unused. These unused slots are ignored by the destination component.

For example, for a 1T2R system, the transmit burst would have two unused slots.

e.g., RFIC captures I, Q, X, X, I, Q, X, X, ...

The unused "X" slots may be filled with arbitrary data values by the BBIC. Such values could be either constant values, or the preceding data sample values can be repeated to reduce the bus switching factor and hence power consumption.

4.2 Data bus idle and turnaround periods

The DIQ[9:0] bus signals are actively driven by the BBIC during a transmit burst and by the RFIC during a receive burst. Between bursts, there is no data being transferred and the data path interface is "idle". During such idle periods, the data bus values are ignored by both components, but to avoid the DIQ[9:0] bus signals floating to invalid levels, the BBIC must either

continuously drive the DIQ[9:0] bus signals to valid levels

or

implement weak-pullups so that the DIQ[9:0] bus signals float to a stable high level.

4.2 Data bus idle and turnaround periods (cont'd)

During idle periods, either or both clock signals may be stopped as described in 4.1.1 and 4.1.2.

The data path transfer bursts are defined with start and finish latencies of two cycles each. The BBIC must allow sufficient time between finishing one burst and starting the next to avoid any possibility of bus contention. Since the BBIC is always driving the DIQ[9:0] bus around a transmit burst, the only possibility for bus contention exists around a receive burst. These possible contention times are captured in the receive burst preamble and postamble times in 4.3.2.

4.3 Data path functional timing

4.3.1 Transmit burst

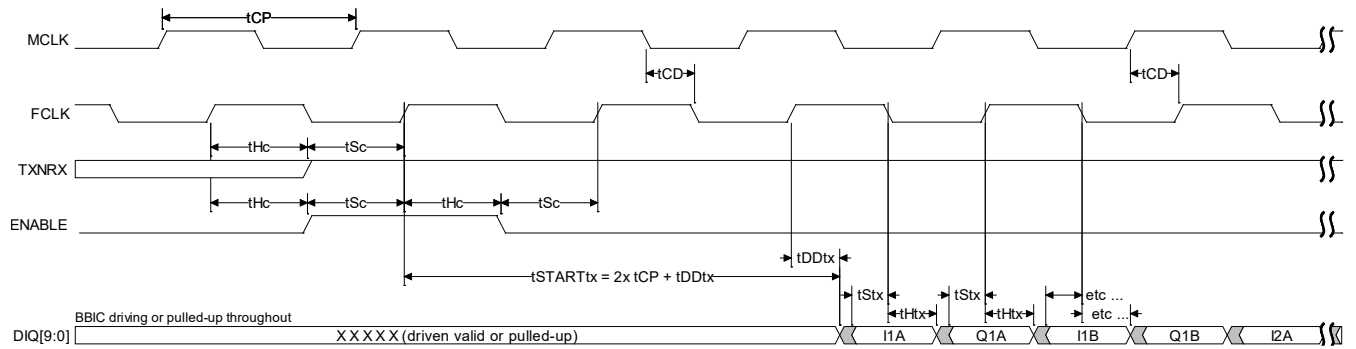


Figure 3 — Data path transmit burst start

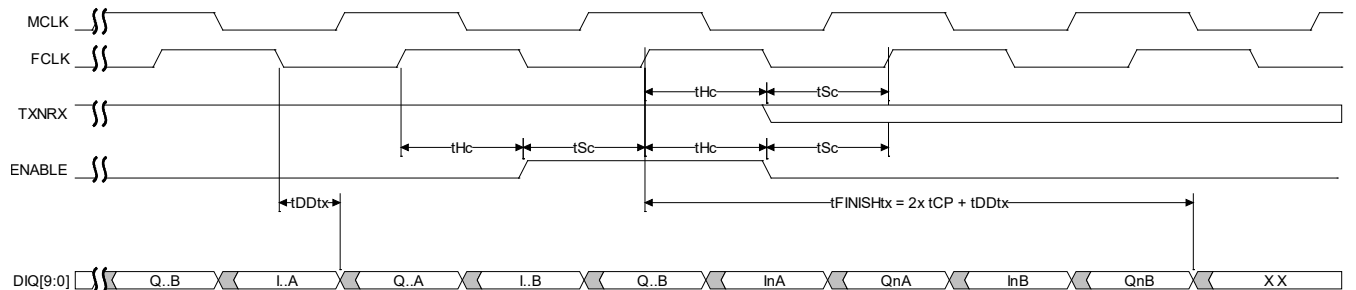


Figure 4 — Data path transmit burst finish

During a transmit burst, the BBIC drives the data values on DIQ[9:0] with a delay offset t_{DDtx} from FCLK. This provides the separation between FCLK edges and transmit data transitions on DIQ[9:0], to ensure that the t_{Stx} and t_{Htx} constraints are met at the RFIC inputs, and allows the RFIC to use FCLK to capture DIQ[9:0].

The transmit burst start latency is measured from the FCLK rising edge at which the RFIC samples ENABLE high to the DIQ[9:0] bus transition presenting the first valid transmit data sample. The transmit burst finish latency is measured from the FCLK rising edge at which the RFIC samples ENABLE high to the DIQ[9:0] bus transition removing the last valid transmit data sample. These latency definitions therefore include the t_{DDtx} transmit data delay offset.

4.3 Data path functional timing (cont'd)

4.3.2 Receive burst

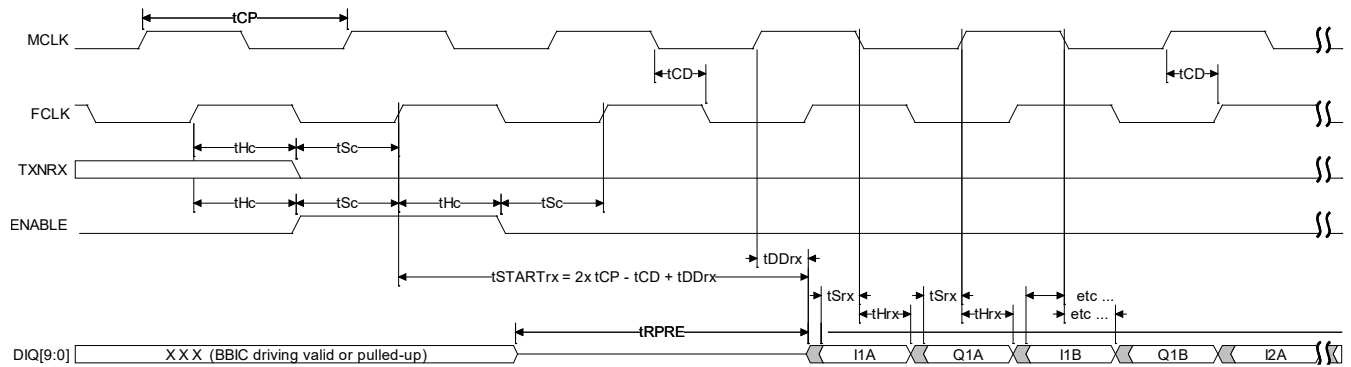


Figure 5 — Data path receive burst start

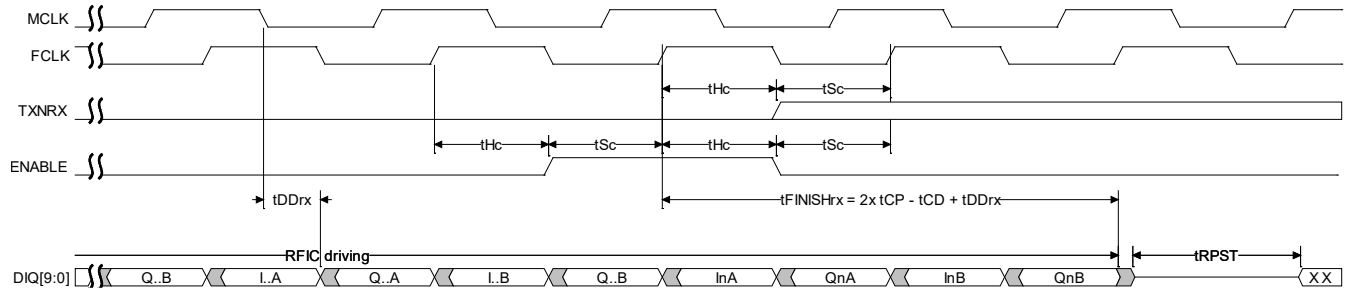


Figure 6 — Data path receive burst finish

During a receive burst, the RFIC drives the data values on DIQ[9:0] with a delay offset t_{DDrx} from MCLK. This provides the separation between MCLK edges and receive data transitions on DIQ[9:0], to ensure that the t_{Srx} and t_{Hrx} constraints are met at the BBIC inputs, and allows the BBIC to use MCLK to capture DIQ[9:0].

The receive burst start latency is measured from the FCLK edge at which the RFIC samples ENABLE high to the DIQ[9:0] bus transition presenting the first valid receive data sample. The receive burst finish latency is measured from the FCLK edge at which the RFIC samples ENABLE high to the DIQ[9:0] bus transition removing the last valid receive data sample. These latency definitions therefore include the t_{DDrx} receive data delay offset. The t_{CD} phase offset between MCLK and FCLK reduces the receive burst start and finish latencies.

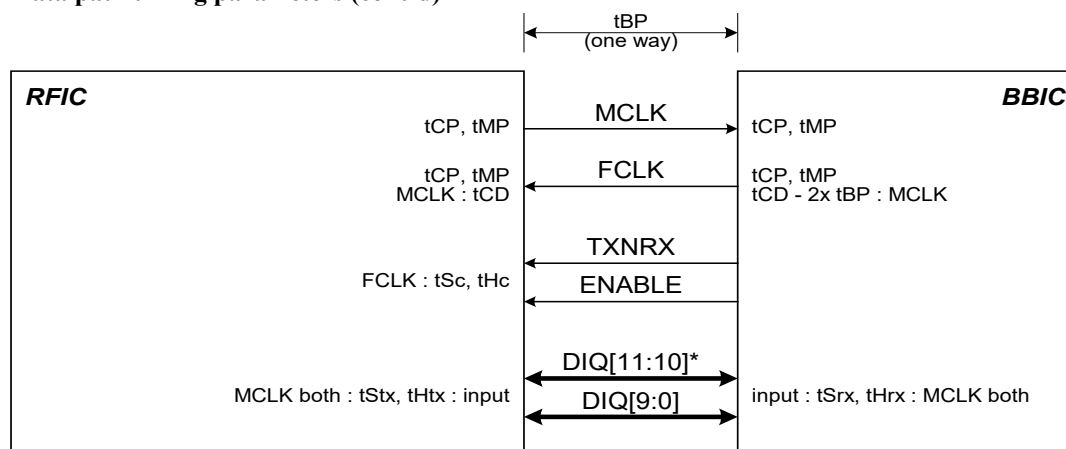
The receive burst preamble time t_{RPRE} and receive burst postamble time t_{RPST} bus turnaround periods must be at least two full clock cycles.

4.3.3 Data path timing parameters

The diagram in Figure 7 shows the fundamental timing constraints which must be satisfied for the data path interface. (For example, the t_{CP} and t_{MP} constraints apply to the RFIC FCLK input independent of other signals, while the t_{CD} constraint applies to the RFIC FCLK input referenced to the RFIC MCLK output.)

4.3 Data path functional timing (cont'd)

4.3.3 Data path timing parameters (cont'd)



* DIQ[11:10] are optional, implemented if support for 12-bit baseband sample widths is required.

Figure 7 — Data path timing constraints summary

The following table gives the values of the timing constraints for the data path interface.

Table 1 — Data path timing constraint values

Parameter	Min	Typical	Max	Description
tCP	11.16 ns			MCLK cycle time (clock period) (typical MCLK frequencies are given in Annex A)
tMP	45% of tCP			MCLK and FCLK high and/or low minimum pulse width (including effects of duty cycle distortion, period jitter, cycle-cycle jitter and half-period jitter)
			200 ps	MCLK and FCLK period jitter (as defined in JESD65) +/- 2½ sigma limits measured over 10 ⁷ clock cycles assuming random jitter with normal/Gaussian distribution
			200 ps	MCLK and FCLK cycle-cycle period jitter (as defined in JESD65) +/- 2½ sigma limits measured over 10 ⁷ clock cycles assuming random jitter with normal/Gaussian distribution
			200 ps	MCLK and FCLK half-period jitter (as defined in JESD65) +/- 2½ sigma limits measured over 10 ⁷ clock cycles assuming random jitter with normal/Gaussian distribution
tBP			1 ns	PCB trace delay between BBIC and RFIC MCLK from RFIC to BBIC FCLK, TXNRX and ENABLE from BBIC to RFIC DIQ[9:0] both ways
tCD	0 ns		45% of tCP	Delay between MCLK output and FCLK input at RFIC (Includes 2x tBP)
tSc	2 ns			Control signal setup time to FCLK at RFIC inputs
tHc	2 ns			Control signal hold time from FCLK at RFIC inputs
tStx	1.3 ns	tCP/4		Tx data setup time to FCLK at RFIC inputs
tHtx	1.3 ns	tCP/4		Tx data hold time from FCLK at RFIC inputs
tSrx	1.3 ns	tCP/4		Rx data setup time to MCLK at BBIC inputs
tHrx	1.3 ns	tCP/4		Rx data hold time from MCLK at BBIC inputs
tRPRE	tSTARTRx - 2x tCP			Time at which BBIC stops driving DIQ[9:0] before a receive burst
tRPST	tFINISHRx + 2x tCP			Time at which BBIC starts driving DIQ[9:0] after a receive burst

These timing parameters are measured as described in 6.5.

5 Control Plane Functional layer

The RBDP control plane interface definition uses a defined serial transaction protocol to send read and write commands and write data from the BBIC to the RFIC and to return read response data to the BBIC. The BBIC is the interface controller, initiating and terminating all control plane transactions.

Control plane transactions consist of a control field and one or more data fields. The control field contains one command bit coded R=1 / Wb = 0 and seven address bits. Each data field contains eight data bits either to be written into or read from the RFIC. The address field and data fields are serially transferred most significant bit first. The transaction formatting and bit ordering are shown in 5.2.

The control plane definition uses a chip select signal to indicate which RFIC is the target of the transaction and to delineate the transaction, and a clock signal to define individual serial bit timeslots on the serial data signals. The data communication may be implemented with two unidirectional signals (giving an interface total of 4 pins, or one bidirectional signal (giving an interface total of 3 pins). The RFIC can implement either one of these options; the BBIC must support both. The BBIC may support both options concurrently or as a hardwired selection at board build time.

The control plane interface signals are conceptually described as point-to-point between the BBIC and RFIC. However if electrical loading and interface timing permit, the clock and data signals could be shared connections with other components not covered by this interface definition.

5.1 Control Plane signals

The control plane interface consists of the following signals.

5.1.1 CPCLK (Driven from BBIC to RFIC)

While the control plane is idle, CPCLK is kept low. During a transaction CPCLK provides 8 high pulses to define the 8-bit control field and Nx 8 high pulses to define the Nx 8-bit data fields (note : N >= 1).

5.1.2 CPCSBB (Driven from BBIC to RFIC)

CPCSBB is driven low before the first CPCLK rising edge, remains low during the whole transaction, and is driven high again after the last CPCLK falling edge. The RFIC ignores the clock and data signals while CPCSBB is high.

If CPCSBB is de-asserted other than on an octet boundary, the control plane transaction will not complete correctly and information may be lost.

A write transaction will complete an internal 8-bit write operation after each data field has been fully received. An incomplete (non-octet) final data field will not trigger a write operation and the bits received by the RFIC in the incomplete data field will be discarded.

A read transaction will complete an internal read operation, along with any side-effects (e.g. clearing clear-on-read status bits) before starting to shift out each data field. Hence, if CPCSBB is de-asserted before the end of a read data field, any remaining read data bits will be discarded by the RFIC; however, side-effects of the preceding internal read operation cannot be done and hence information may be lost.¹),

¹ The use of clear-on-write-1-per-bit status bits is recommended.

5.1 Control Plane signals (cont'd)

5.1.3 CPSDO, CPSDI and CPDIO

Two unidirectional data signal option

CPSDO : Driven from BBIC to RFIC

CPSDI : Driven from RFIC to BBIC

Single bidirectional data signal option

CPDIO : Bidirectional

The data signals are launched on the rising edge of CPCLK and sampled on the falling edge of CPCLK by both BBIC and RFIC.

CPSDO or CPDIO carry the Command/Address field from BBIC to RFIC during all transactions, and the write data fields during a write transaction. CPSDI or CPDIO carry the returning read data fields from RFIC to BBIC during a read transaction.

Data signals which are unused for some periods of time must not float undriven. Such cases include :

the CPSDO signal during the data field(s) of a read transaction

the CPSDI signal during the control field of any transaction and the data field(s) of a write transaction

both CPSDO and CPSDI, or CPDIO, between transactions

It is recommended to implement weak pull-ups on the data signal either at the BBIC or on the PCB, but not at the RFIC².

² This point avoids precluding the use of a multi-drop wired-AND data signal topology.

5.2 Control plane functional timing

5.2.1 Single transactions

In these diagrams, timing relationships are shown both for chip inputs (e.g. setup and hold times) and for chip outputs (e.g. output propagation times). The signal CPCLK(s) and delay tCO(s) are explicitly identified for the client side of the interface, to illustrate the effects of board propagation delays on the clock going from BBIC to RFIC and the data going from RFIC to BBIC. The AC timing parameter values are specified in section 5.2.3.

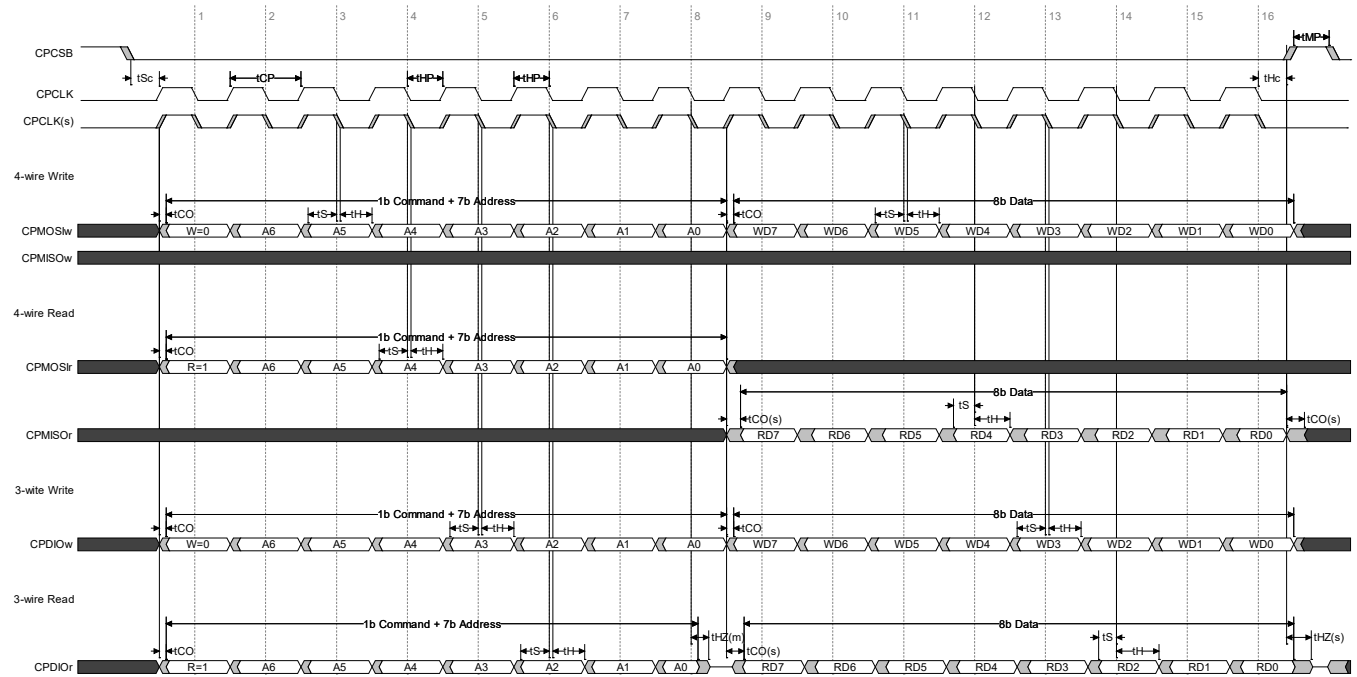


Figure 8 — Control plane 4-wire and 3-wire single transactions

5.2 Control plane functional timing (cont'd)

5.2.2 Extended data transactions

Extended data transactions, transferring multiple data fields with a single command/address field, may be implemented optionally by both RFIC and BBIC.

An extended data transaction involves more than one data field being transferred contiguously after the first data field in the transaction, and can consist either of multiple writes or of multiple reads. Writes and reads cannot be mixed in a single extended transaction.

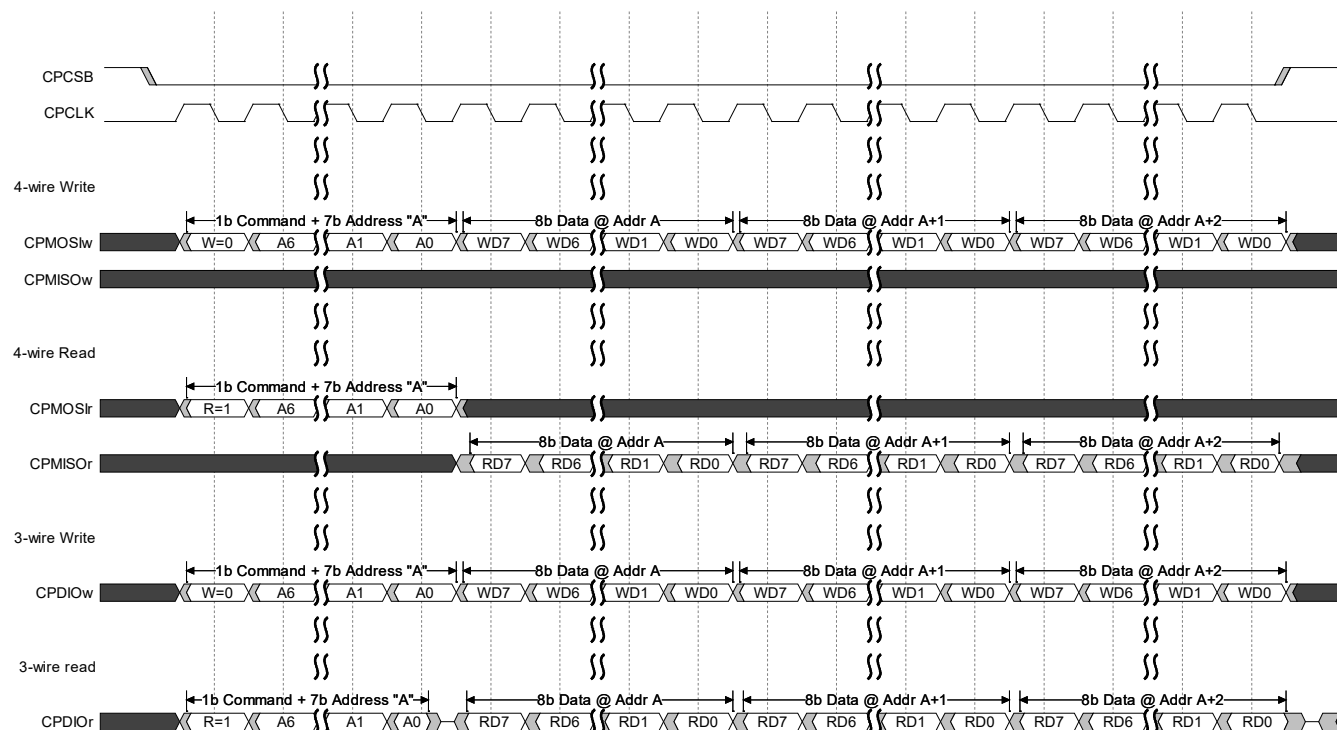


Figure 9 — Extended transactions with 3 data fields

The first data field is transferred using the address specified in the transaction command/address field. Each subsequent data field is mapped to incrementing address locations. If the incrementing address exceeds the maximum address space implemented within the RFIC, it is wrapped to 0x0 and the incrementing sequence continues thereafter. The BBIC must handle this wrapping or avoid it by controlling the number of data fields included in any given transaction.

The control plane throughput and latency figures resulting from various extended transaction lengths are given in Table 2. The table demonstrates the diminishing returns as the extended transaction length limit increases towards eight data fields. To bound implementation cost, a maximum of eight data fields is recommended. Either RFIC or BBIC may implement a lower maximum transaction length than this recommended figure.

5.2 Control plane functional timing (cont'd)

5.2.2 Extended data transactions (cont'd)

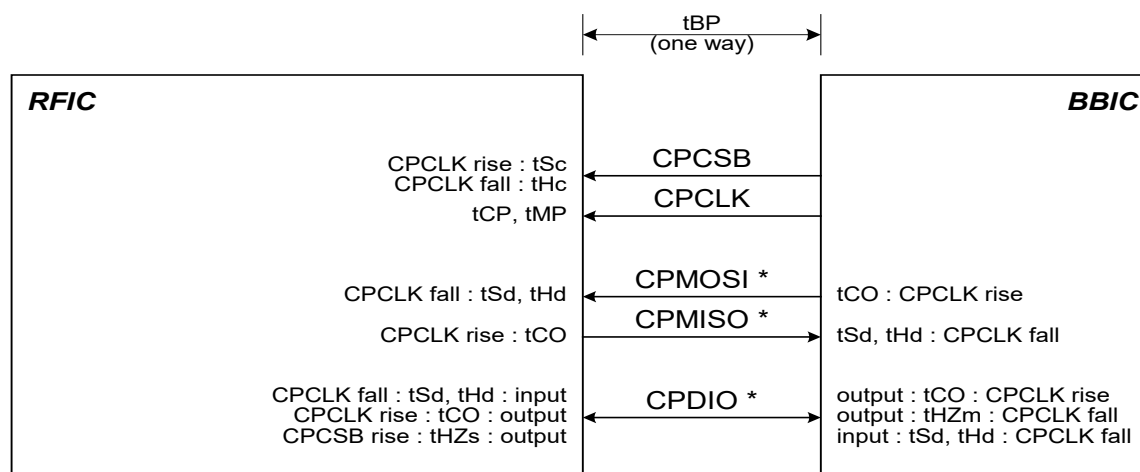
Table 2 — Control plane extended data transaction performance gains

Cmnd+Addr bytes	Data bytes	Total bytes	Data utilization efficiency	Transaction duration (ns) for 50MHz CPCLK	Data rate (Mbps) for 50MHz CPCLK
1	1	2	50%	325	24.6
1	2	3	67%	485	33.0
1	3	4	75%	645	37.2
1	4	5	80%	805	39.8
1	5	6	83%	965	41.5
1	6	7	86%	1125	42.7
1	7	8	88%	1285	43.6
1	8	9	89%	1445	44.3

It is not necessary to always use the longest possible transaction. Each individual transaction can be any length in the range supported by a given RFIC/BBIC pair. This allows the optimization of bandwidth or transaction latency as required on a per-transaction basis.

5.2.3 Control plane timing parameters

The diagram in shows the fundamental timing constraints which must be satisfied for the control plane interface. (For example, the tCP and tMP constraints apply to the RFIC CPCLK input independent of other signals, while the tSc and tHc constraints apply to the RFIC CPCSBB input referenced to the RFIC CPCLK input.)



* The serial data transfer may be implemented using a single bidirectional pin CPDIO instead of two unidirectional pins CPMOSI and CPMISO.

Figure 10 — Control plane timing constraints summary

5.2 Control plane functional timing (cont'd)

5.2.3 Control plane timing parameters (cont'd)

The following table gives the value of the timing constraints for the control plane interface.

Table 3 — Control plane timing constraint values

Parameters	Min	Typical	Max	Description
tCP	20 ns			Control Plane clock period <i>See section 5.3 below for required clock division ranges</i>
tMP	9 ns			Clock min pulse width (= 45% duty cycle for 20ns period) Also applies to the minimum de-assertion time for CPCSBB between transactions.
tBP			1 ns	PCB trace delay between BBIC controller and RFIC client CPCSBB and CPCLK from BBIC to RFIC CPSDO or CPDIO from BBIC to RFIC CPSDI or CPDIO from RFIC to BBIC
tSc	6 ns			Setup time from CPCSBB assertion to first CPCLK rising edge
tHc	10 ns			Hold time from last CPCLK falling edge to CPCSBB de-assertion
tSd	1.5 ns			CPSDO/CPSDI or CPDIO data input setup time against CPCLK
tHd	1.5 ns			CPSDO/CPSDI or CPDIO data input hold time against CPCLK
tCO	2 ns		5.5 ns	Derived constraint Clock edge to output data change CPCLK input to CPSDI output or CPDIO output for RFIC CPCLK output to CPSDO output or CPDIO output for BBIC
tHZm	tHd		tCO(max)	Derived constraint In a read transaction, BBIC must stop driving the last address bit on CPDIO before RFIC drives the first read data bit
tHZs	0 ns		tCO(max)	In a read transaction, RFIC stops driving the last read data bit on CPDIO after CPCSBB deassertion

These timing parameters are measured as described in 6.5.

5.3 Control plane clock frequency bands

The BBIC may support a maximum CPCLK frequency in the range $1/tCP(\min)$ down to $\frac{1}{2}$ that rate. The BBIC must also support division of the highest CPCLK frequency by factors of 2 and 4. Thus, a specific BBIC must support a CPCLK frequency in each of the three bands :

50 - 25 MHz
25 - 12.5 MHz
12.5 - 6.25 MHz

The BBIC may also support lower frequencies than these bands, and may support dynamic changes to the control plane clock frequency during operation.

The RFIC must support a maximum CPCLK frequency in one of the three bands:

50 - 25 MHz
25 - 12.5 MHz
12.5 - 6.25 MHz

depending upon the RFIC's control plane throughput requirements to support normal operation. The RFIC may also support control plane operation at lower than the implementation-dependent maximum frequency, and may also support dynamic changes to the control plane clock frequency during operation.

6 Electrical layer

The RBDP interface definition uses full-swing LVCMOS single-ended signals. Both the data path and the control plane use nominally point-to-point PCB trace connection topologies. Board-level termination schemes are not required by this interface definition, but may be recommended by RFIC or BBIC component vendors.

6.1 Absolute maximum ratings

Table 4 — Absolute maximum ratings

Parameters	Rating
Supply voltage, Vdd	-0.5V to 2.5V
Signal voltage, Vio	-0.5V to Vdd+0.5V, not to exceed 2.5V

Exceeding these absolute maximum ratings may result in damage to the component. Normal operation is not implied under these conditions.

6.2 Normal operating conditions

Table 5 — Normal operating conditions

Parameters	Min	Typical	Max	Description
Vdd (dp)	1.71V	1.80V	1.89V	IO driver Supply voltage (data path)
Vdd (cp)	1.71V		2.5V	IO driver Supply voltage (control plane)
Vio	0V		Vdd	Voltage applied to signal pins

Correct component operation shall be guaranteed within the range of normal operating conditions.

The control plane signaling supply voltage may work off either a 1.8V supply or a 2.5V supply. This standard permits but does not require RFICs and BBICs to implement 2.5V signaling for the control plane.

6.3 DC characteristics

Table 6 — DC characteristics

Symbol	Parameters	Min	Max	Unit
Vih	Input high voltage	0.65Vdd	Vdd + 0.3	V
Vil	Input low voltage	-0.3	0.35Vdd	V
Voh	Output high voltage while drawing 2mA shorted to 0V	Vdd – 0.45		V
Vol	Output low voltage while drawing 2mA shorted to Vdd		0.45	V
Ii	Input leakage current		+/- 10	uA

It is recommended that the IO circuit designs consume zero supply current when in the sleep state.

6 Electrical layer (cont'd)

6.4 AC characteristics

Table 7 — AC characteristics

Symbol	Parameters	Min	Max	Unit
Ci	Input capacitance		5	pF
Is	Input slew rate measured between Vil and Vih	0.7		V/ns

This minimum input slew rate must be ensured by the source chip's drivers within the PCB design envelope described in Annex C. The quoted figure is required to ensure timing closure at the highest interface rate. System designs which do not require the highest interface rate may tolerate components which provide lower slew rates, with possible benefits in system noise reduction.

6.5 Timing parameter measurement

The timing parameters quoted in 4.3.3 and 5.2.3 are measured from the latest Vil/Vih crossing point on the earlier-changing signal to the earliest Vih/Vil crossing point on the later-changing signal. This is illustrated conceptually for clock-vs-data setup and hold times in Figure 11 below where both clock and data³ are inputs, but also applies to all other timing parameter measurements such as clock pulse width checks, input-to-output constraints and output-to-output constraints, as well as the data path MCLK-to-FCLK loop delay parameter tCD.

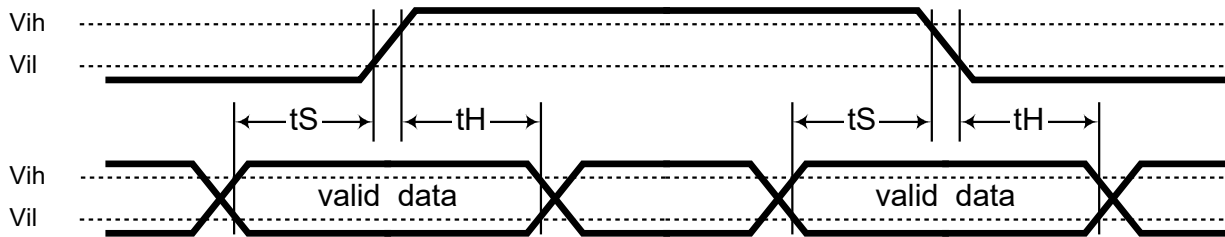


Figure 11 — Timing parameter measurement

This definition of timing parameters allows for implementation-dependent optimizations in electrical performance (e.g., slew rate of outputs, and PCB signal integrity) and trade-offs with internal logic delays in meeting interface timing requirements.

³ “data” in this case also includes the data path burst control TXNRX & ENABLE signals and control plane CPCSB signal

Annex A Data path applications and resulting sample/data/clock rates

This Annex illustrates some example applications of the data path interface and the resulting baseband complex sample rates, interface data rates and clock rates. When reading these tables, note that two interface data words (i.e., an I & Q pair of samples, constituting a single complex baseband sample value) are transferred per MCLK or FCLK cycle.

A.1 Mandatory rates

In Table 8 below, both of the “20 MHz channel bandwidth” rows are optional.

Table 8 — Mandatory interface rates : 2T2R or 1T2R, 2x Fs

MIMO 2T2R or 1T2R system ; 2x Nyquist sampling

Radio Channel Bandwidth (MHz)	802.16 Sampling Factor	802.16 (complex) Fs Sampling Frequency (MSps)	Fs multiplier (I&Q ; 2x arms AND 2x over-sampling)	Interface aggregate data sample rate (Mps)	Interface data sample period (ns)	MCLK & FCLK (MHz)
20.00	28/25	22.40	8	179.20	5.58	89.60
10.00	28/25	11.20	8	89.60	11.16	44.80
8.75	8/7	10.00	8	80.00	12.50	40.00
7.00	8/7	8.00	8	64.00	15.63	32.00
5.00	28/25	5.60	8	44.80	22.32	22.40
3.50	8/7	4.00	8	32.00	31.25	16.00
20.00	802.11n : n/a	20.00	8	160.00	6.25	80.00

Table 9 — Mandatory interface rates : 1T1R, 2x Fs

SISO 1T1R system ; 2x Nyquist sampling

Radio Channel Bandwidth (MHz)	802.16 Sampling Factor	802.16 (complex) Fs Sampling Frequency (MSps)	Fs multiplier (I&Q ; 2x over-sampling)	Interface aggregate data sample rate (Mps)	Interface data sample period (ns)	MCLK & FCLK (MHz)
20.00	28/25	22.40	4	89.60	11.16	44.80
10.00	28/25	11.20	4	44.80	22.32	22.40
8.75	8/7	10.00	4	40.00	25.00	20.00
7.00	8/7	8.00	4	32.00	31.25	16.00
5.00	28/25	5.60	4	22.40	44.64	11.20
3.50	8/7	4.00	4	16.00	62.50	8.00
20.00	802.11n : n/a	20.00	4	80.00	12.50	40.00

A.2 Optional rates

Table 10 — Optional interface rates : 2T2R or 1T2R, 1x Fs

MIMO 2T2R or 1T2R system ; 1x Nyquist sampling

Radio Channel Bandwidth (MHz)	802.16 Sampling Factor	802.16 (complex) Fs Sampling Frequency (MSps)	Fs multiplier (I&Q ; 2x arms)	Interface aggregate data sample rate (Msps)	Interface data sample period (ns)	MCLK & FCLK (MHz)
20.00	28/25	22.40	4	89.60	11.16	44.80
10.00	28/25	11.20	4	44.80	22.32	22.40
8.75	8/7	10.00	4	40.00	25.00	20.00
7.00	8/7	8.00	4	32.00	31.25	16.00
5.00	28/25	5.60	4	22.40	44.64	11.20
3.50	8/7	4.00	4	16.00	62.50	8.00
20.00	802.11n : n/a	20.00	4	80.00	12.50	40.00

Table 11 — Optional interface rates : 1T1R, 1x Fs

SISO 1T1R system ; 1xNyquist sampling

Radio Channel Bandwidth (MHz)	802.16 Sampling Factor	802.16 (complex) Fs Sampling Frequency (Msps)	Fs multiplier (I&Q)	Interface aggregate data sample rate (Msps)	Interface data sample period (ns)	MCLK & FCLK (MHz)
20.00	28/25	22.40	2	44.80	22.32	22.40
10.00	28/25	11.20	2	22.40	44.64	11.20
8.75	8/7	10.00	2	20.00	50.00	10.00
7.00	8/7	8.00	2	16.00	62.50	8.00
5.00	28/25	5.60	2	11.20	89.29	5.60
3.50	8/7	4.00	2	8.00	125.00	4.00
20.00	802.11n : n/a	20.00	2	40.00	25.00	20.00

Annex B (Informative) Description of TXNRX and ENABLE burst control signaling

The ENABLE input used in conjunction with the TXNRX input steps an internal state machine through the operational states of the RFIC. There are three basic states of operation; ALERT STATE, RECEIVE STATE and TRANSMIT STATE. Additional states allowing for transitioning in and out of ALERT STATE can be defined. The definition of the additional states is outside the scope of the standard and will be implementation dependent.

The device transitions from one state to the next state based on the level of TXNRX and ENABLE inputs.

Upon power-up, the RFIC comes up in an initial state (implementation specific state). After device specific start-up time for calibration and configuration, the RFIC is placed in ALERT STATE by a control plane write. From the ALERT STATE, the device can be placed in either the RECEIVE STATE or TRANSMIT STATE by setting the state of TXNRX and ENABLE inputs.

On setting the TXNRX input low and asserting the ENABLE input for one FCLK cycle, the RFIC transitions from the ALERT STATE to the RECEIVE STATE. The data bus DIQ[9:0] is configured as an output from the RFIC, and data is available in the third clock cycle after the ENABLE pulse has been sampled. At the end of the burst, the ENABLE input is again asserted for one FCLK cycle transitioning the device into ALERT STATE. Transitioning to ALERT State keeps the device ready for TRANSMIT or RECEIVE operation.

On setting the TXNRX input high and asserting the ENABLE input for one FCLK cycle, the RFIC transitions from ALERT STATE to the TRANSMIT STATE. The data bus DIQ[9:0] is configured as an input to the RFIC, and data is available in the third clock cycle after the ENABLE pulse has been sampled. At the end of the burst, the ENABLE input is again asserted for one FCLK cycle transitioning the device into ALERT STATE. Transitioning to ALERT STATE keeps the device is ready for TRANSMIT or RECEIVE operation.

The ENABLE and TXNRX inputs are source synchronous relative to FCLK and are required to meet appropriate setup and hold timing relative to the FCLK input. The TXNRX input may be set high or low some number of FCLK cycles (e.g. three) before the ENABLE start pulse.

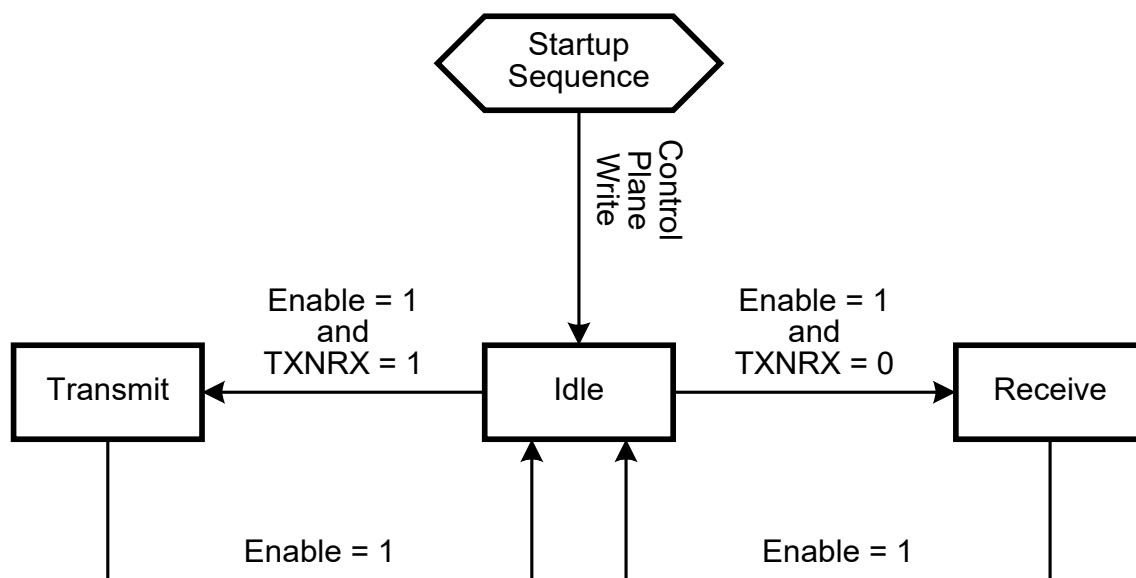


Figure 12 — TXNRX/ENABLE conceptual FSM

B.1 Pulse synchronization fault recovery

The data path interface burst control signaling scheme requires the RFIC to perfectly track the sequence of ENABLE pulses generated by the BBIC. In the event that the RFIC loses synchronization with the ENABLE pulse train, the data path interface will be non-functional until the RFIC regains synchronization. Two possible recovery schemes are identified here.

Automatic hardware recovery

If the RFIC detects a transition on TXNRX during a transfer burst (i.e. between the start and finish ENABLE pulses), the RFIC may terminate the burst and reset its internal pulse-tracking mechanism. The BBIC is not required to cause TXNRX to transition between bursts, but may choose to do so to improve the robustness of the interface.

Control plane polling

If the RFIC provides control-plane visibility of its pulse-tracking FSM, the BBIC may choose to poll this state, and implement a recovery scheme in control plane firmware.

Annex C Recommended PCB trace characteristics and component slew rates

This specification does not explicitly define required driver characteristics. Instead, the necessary driver characteristics are implied by the requirement to ensure a minimum input slew rate at the destination component's input pins within the specified envelope of PCB trace characteristics given in the table below.

Table 12 — PCB trace characteristics

Parameters	Min	Max	Unit
PCB trace length	0	6	inch
PCB trace impedance	50	70	Ohm
Series Termination Resistance (optional)	0	40	Ohm
PCB trace propagation delay mismatch between related signals		70	ps

The use of a series termination resistor is optional; if present, it is recommended to be placed as close as possible to the RFIC.

The RFIC may specify use of the series termination resistor to reduce the output slew rate of its drivers to control RFIC-internal noise generation (while still ensuring the minimum input slew rate is met at the BBIC inputs). The RFIC may specify a narrower range of resistance values than the nominal range given above (for example, a given RFIC might require a resistance in the range 10-30 Ohm).

If not actually required by the RFIC, the series termination resistor may still be used in some PCB designs to ensure adequate signal integrity on longer PCB traces. To support this case, the RFIC should specify what values of series termination resistor it can tolerate to ensure the minimum input slew rate for the BBIC.

The BBIC should be designed to support any value of series termination resistor in the range in the table above.

It is also recommended that both the RFIC and BBIC components provide programmable drive strengths for their output drivers. This will allow the signal transition times and slew rates to be optimized to meet timing requirements while edge rates and resulting electrical noise generation are minimized, reducing consequent requirements for shielding and/or decoupling to mitigate such noise.

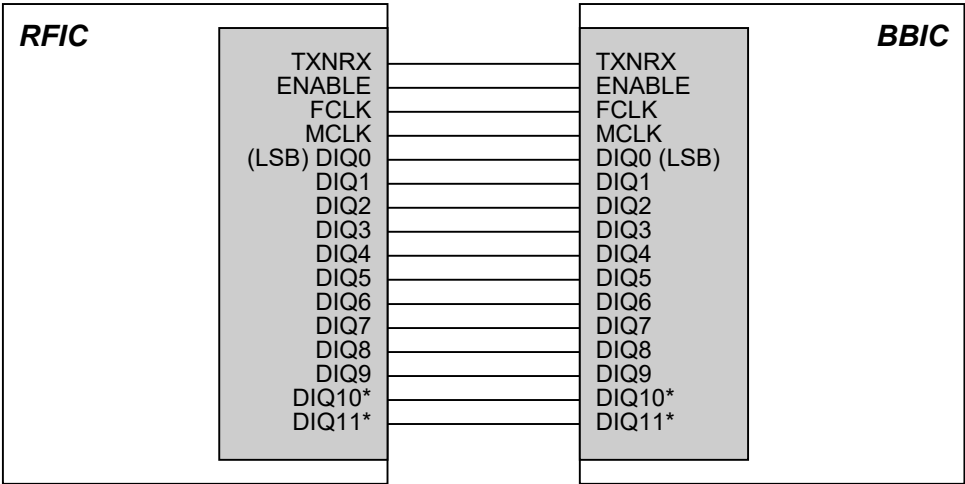
Annex D Recommended component pin ordering

It is recommended (but not mandatory) that packaged BBIC and RFIC devices adhere to the following specified pin ordering where the high speed signals are driven off a single row of pins/solder balls at the package edge.

The intent of this is to encourage a compact, low parasitic PCB layout where the data bus and synchronization signals are not twisted and the propagation delays are closely matched.

It is recommended that the data path signals DIQ[11:10] (where applicable), DIQ[9:0], MCLK, FCLK, ENABLE and TXNRX shall be pinned out in a contiguous group on the periphery of the BBIC and RFIC packages (aside from power and ground pins which may be interposed as required). It is further recommended that the pins shown be located on a single edge of each package.

It is recommended that the pin ordering shall be as shown in the figure below, looking down on the packaged components on the PCB from above:



* DIQ[11:10] are optional, implemented if support for 12-bit baseband sample widths is required.

Figure 13 — Recommended BBIC/RFIC pin ordering

The control plane signals passing between the BBIC and RFIC do not require a specified pinout and can be allocated without restriction on both components.



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